UNITED STATES PATENT AND TRADEMARK OFFICE

14

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,421	05/25/2001	Takahisa Yamaha	P/2171-195 DIV	6324

7590 05/27/2004

Steven I Weisburd Esq
Dickstein Shapiro Morin & Oshinsky LLP
1177 Avenue of the Americas-41st Floor
New York, NY 10036-2714

EXAMINER	
NGUYEN, HA T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/866,421	YAMAHA, TAKAHISA	
	Examiner	Art Unit	
	Ha T. Nguyen	2812	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-40* is/are allowed.

6)☒ Claim(s) *14,15,19-26,30-34 and 41-52* is/are rejected.

7)☒ Claim(s) *16-18 and 27-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notice to applicant

1. Applicant' s Amendment, Response to the Office Action mailed 11-18-03 and request for an RCE have been entered and made of record. Following is an Office Action responding to the request.

Claim Objections

2. Claims 41-43 are objected to because of the following informalities: In claims 41-43, lines 2, substitution of "sidewall lamination" with --conductive portion--is suggested for correctness. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 14, 15, 19-26, 30-34 and 41-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (USPN 5739587) in view of Shiue et al. (USPN 5923088, hereinafter "Shiue") and Huang et al. (USPN 6265313, hereinafter "Huang").

[Re Claims 23, 24, 34, and 41-52] Referring to Figs. 11-19 and 23A, Sato discloses a method of manufacturing a semiconductor device, the method comprising: (a) forming an

insulating film 20 on a semiconductor substrate 10; (b) forming a first conductive pad 550 on the insulating film; (c) forming a first interlayer insulating film 540 on the first conductive pad and the insulating film; (d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film(see Fig. 15); (e) filling the plurality of first though holes with conductive material 611-616; (f) simultaneously forming a second conductive pad 530 and a second wiring layer 1110 on the first interlayer insulating film, each of the second conductive pad and the second wiring layer being in contact with the conductive material in the plurality of first through holes (see Figs. 15 and 16); (g) forming a second interlayer insulating film 520 on the second conductive pad, the second wiring and the first interlayer insulating film; (h) forming a plurality of second through holes in the second interlayer insulating film, each of the second through holes extending from the second conductive pad or the second wiring layer, respectively, to an upper surface of the second interlayer insulating film (see Fig. 15);(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material 601-606 (see Figs. 15 and 16); (j) simultaneously forming a third conductive pad 510 and a third wiring layer 1100 on the second interlayer insulating film, each of the third conductive pad and wiring layer being in contact with the conductive material in one or more of the second through holes formed in the second interlayer insulating film;(k) forming a third interlayer insulating film 500 on the third conductive pad , the third wiring layer and the second interlayer insulating film;(l-1) forming a through hole through the third interlayer insulating; and (m) forming a bonding pad on the third conductive pad in the through, hole in the third interlayer insulating film(see Fig. 23A); forming simultaneously a first conductive pad and a first wiring layer on the insulating layer; [Note that the first level corresponds to the base level of claim 24, the second level corresponds to an intermediate level, and the third level correspond to the upper level of claim 24];[Re Claims 14 and 25] (d) forming a passivation film 9400 on the insulating film of the upper layer, the passivation film exposing the bonding pad (see Fig. 23A); [Re Claims 19 and 30] wherein the step (e) or (b)(4) comprises: forming Ti films 4000 covering an inner surface of the through holes in the insulating film of the base layer (see Fig. 16); forming TiN layers 4100 on the Ti films; and forming W layers 5000 on the TiN layers. But it does not disclose expressly that the through hole through the third interlayer insulating film is substantially the same size as the third

conductive pad, the simultaneous formation of wiring layer and conductive pad in level other than the first and second level and the formation of conductive portion covering a side wall of the through hole through the third interlayer insulating film so that part of the third conductive pad is exposed, the conductive portion being formed by forming a conductive layer including Ti, TiN covering the entire side wall then etching the conductive layer. However, the missing limitation are well known in the art because Shiue discloses s opening substantially the same size as the conductive pad (See Fig. 3) and Huang discloses the forming of a conductive spacer 322 by depositing metal layers then etching (see Fig. 3G and related text). A person of ordinary skill is motivated to modify Sato with Shiue and Huang to obtain better contact between the bonding wire (test fixture) and more reliable device. The combined teaching of Sato, Shiue and Huang does not disclose Ti/TiN/W conductive layer on a side wall. However Sato discloses the use of conductor having said combination, as shown above. Besides, it would have been obvious for a person of ordinary skill in the art to simultaneously form conductive pad and wiring in as many layers as needed ensuring a faster and lower manufacturing cost.

[Re Claims 15 and 26] the combined teaching discloses substantially the limitations of claims 15 and 26. But it does not discloses that the passivation film is formed by forming a silicon oxide film and a silicon nitride film. However, the examiner takes Official Notice that it is well known in the art that a composite layer of silicon oxide and silicon nitride is used as passivation layer to obtain resistance against moisture and scratch.

[Re Claims 20 and 31] wherein the step (e) or (b)(4) comprises: forming Ti films covering an inner surface of the through holes in the insulating film of the base layer; forming TiN layers on the Ti films; and forming W layers on the TiN layer. argument similar to the argument for the rejection of claims 19 and 30. But it does not disclose the use of sputtering to deposit Ti and TiN. However sputtering is commonly used to deposit Ti and TiN for better adhesion.

[Re Claims 21 and 32] wherein the step (e) or (b)(4) comprises: forming Ti covering an inner surface of the through holes in the insulating film of the base layer; forming TIN layers on the Ti films; and w forming W layers on the TiN layer by blanket deposition (see fig. 16). But it does not disclose the use of CVD to deposit W. However CVD is commonly used to deposit W to obtain better step coverage.

[Re Claims 22 and 33] wherein the step (b) or (b)(1) of forming the conductive pad comprises: forming a Ti layer 4000a ; forming an Al-Cu alloy layer 1210; forming a Ti layer4000a, and forming a TIN layer 1212(see Fig. 18).

Therefore, it would have been obvious to combine Sato with Shiue to obtain the invention as specified in claims 14, 15, 19-26, 30-34 and 41-52.

Allowable Subject Matter

5. Claims 16-18 and 27-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcoming the rejection under 35 U.S.C. 112, second paragraph.

Claims 35-40 are allowed.

Claims 16, 27, 35, and 38 recite the steps of: forming a silicon oxide film; coating hydrogen silsesquioxane resin on the silicon oxide film; thermally treating the hydrogen silsesquioxane to form a first ceramic silicon oxide film; and forming a thick silicon oxide film on the first silicon oxide film by plasma CVD.

These features in combination with the other elements of the claims are neither disclosed nor suggested by the prior art of record.

Claims 17, 18, 28, 29, 36, 37, 39, and 40 variously depend from claims 16, 27, 35, or 38, they are allowed for the same reason.

Response to Amendment

6. In view of Applicants' amendment to the claims, the allowability of claims 14-15, 19-26, and 30-34 as stated in the Office Action mailed 11-18-3, has been withdrawn.

New ground of rejection has been provided as shown above.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha Nguyen whose telephone number is (571) 272-1678. The

examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Neibling, can be reached on (571) 272-1679. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Ha Nguyen
Primary Examiner
5-24 - 04